REMARKS

The above amendments delete the originally filed claims in prior application 09/169,736 and add non-elected claims formerly pending in prior application 09/169,736.

No fee is believed to be due with this amendment. However, should the commissioner determine otherwise, he is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 16-1150 (Order No. 009797-0085-999) for any matter in connection with this response, which may be required.

Respectfully submitted,

Date: December 11, 2001

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APPENDIX A

Changes to the Specification

Insert the following Section Title and paragraph on page, line 1, just after the title:

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of prior U.S. Patent Application Serial No. 09/169,736, filed October 09, 1998, which is incorporated herein in its entirety.

Rewrite the paragraph starting on page 17, line 20, as follows:

As can be seen in Fig. 4, no resource conflicts are observed in the case where a write operation follows another write operation (e.g., write operations 400 and 405). Moreover, data can also be efficiently transferred in the case where a write operation follows a read operation (e.g., read operation 410 and write operation 415). This is because the read data can be followed immediately with write data. Although not illustrated in Fig. 4, the case where a read operation is followed by another read operation also experiences no resource conflicts. These combinations fail to experience such conflicts because the data transfer requested by the given operations are not in contention for the same resources. For example, write data 425 is transferred from data signal lines 114 to column I/O lines 266 before write data 430 needs data signal lines 114. Thus, no resource conflict occurs.

Rewrite the paragraph starting on page 26, line 12, as follows:

The highlighted read operation in Fig. 10 shows the read control being transmitted on control signal lines 112, which causes the memory core to be controlled by signals 710 and 715. The characteristics of memory core 180 affect

the time at which the read data is available and delivered via signals 775, which are transmitted from the memory device on data signal lines 114.